

SEMICONDUCTOR DEVICE, SEMICONDUCTOR PACKAGE, ELECTRONIC  
DEVICE, ELECTRONIC APPARATUS, AND MANUFACTURING METHODS OF  
SEMICONDUCTOR DEVICE AND ELECTRONIC DEVICE

RELATED APPLICATIONS

**[0001]** This application claims priority to Japanese Patent Application No. 2003-081221 filed March 24, 2003 which is hereby expressly incorporated by reference herein in its entirety.

BACKGROUND

**[0002]** Field of the Invention

**[0003]** The present invention relates to a semiconductor device, a semiconductor package, an electronic device, an electronic apparatus, and manufacturing methods of the semiconductor device and the electronic device, and particularly to a layered structure such as the semiconductor package.

**[0004]** Description of the Related Art

**[0005]** In a conventional semiconductor device, in order to realize three-dimensional mounting of a semiconductor chip, there has been a method of stacking a package in which the semiconductor chip is mounted through metal balls, as disclosed in Japanese laid-open patent application No. 11-307717.

**[0006]** However, when a semiconductor chip is mounted on a

package, a difference in coefficient of linear expansion or the like between the semiconductor chip and the package causes warping. Therefore, the method of stacking packages through metal balls has had a problem in that the warping caused in the package results in non-uniformity in the interval between packages, which deteriorates the joining strength of the metal balls, thereby leading to deterioration of connection reliability in three-dimensional mounting.

**[0007]** Accordingly, an object of the present invention is to provide a semiconductor device, a semiconductor package, an electronic device, and an electronic apparatus capable of enhancing connection reliability in three-dimensional mounting while considering warping of packages, and manufacturing methods of the semiconductor device and the electronic device.

#### SUMMARY

**[0008]** In order to solve the above-described problem, a semiconductor device according to one embodiment of the present invention comprises: a first semiconductor package, in which a plurality of first joining points are formed, the first joining points having different areas for each of the protruding electrodes; and a second semiconductor package, in which a plurality of second joining points are formed, the second joining points having different areas for each of the protruding electrodes and being arranged so as to be opposed to the respective first joining points.

**[0009]** With this configuration, expansion of the protruding electrodes can be suppressed by both the first joining points and the second joining points, and a thickness of the protruding electrodes joined between the first joining

points and the second surfaces can be adjusted. Therefore, even if there is non-uniformity in the interval between the first semiconductor package and the second semiconductor package, constrictions of the protruding electrodes can be suppressed and connection reliability between the first semiconductor package and the second semiconductor package can be enhanced.

**[0010]** According to one embodiment of the semiconductor device of the present invention, the areas of each of the joining points are opening areas of an insulating layer on lands, with which the protruding electrodes are joined. By changing an opening pattern of the insulating layer that is formed on the lands, the areas of the protruding electrodes can be changed, so that the thickness of the protruding electrodes joined between the first joining points and the second joining points can be adjusted without complicating the manufacturing process.

**[0011]** Furthermore, according to one embodiment of the semiconductor device of the present invention, the areas of each of the joining points are gradually changed from a central portion toward an outer peripheral portion of the semiconductor packages. Therefore, even if one or both of the first semiconductor package and the second semiconductor package warp, the protruding electrodes can be joined between the first joining points and the second joining points while suppressing constrictions of the protruding electrodes.

**[0012]** Furthermore, according to one embodiment of the semiconductor device of the present invention, as an interval between the first semiconductor package and the second semiconductor package becomes

larger, the areas of the first joining points and the areas of the second joining points gradually become smaller. Therefore, in a region where the interval between the first semiconductor package and the second semiconductor package is large, expansion of the protruding electrodes can be suppressed by both the first joining points and the second joining points, and the protruding electrodes can be rendered thick between the first semiconductor package and the second semiconductor package. Accordingly, even if one or both of the first semiconductor package and the second semiconductor package warp, constrictions of the protruding electrodes between the first semiconductor package and the second semiconductor package can be suppressed and connection reliability between the first semiconductor package and the second semiconductor package can be enhanced.

**[0013]** Furthermore, according to one embodiment of the semiconductor device of the present invention, volumes of each of the protruding electrodes joined to the plurality of joining points are substantially the same. Therefore, even if one or both of the first semiconductor package and the second semiconductor package warp, constrictions of the protruding electrodes can be suppressed without changing the sizes of the protruding electrodes, and connection reliability between the first semiconductor package and the second semiconductor package can be enhanced without deteriorating production efficiency.

**[0014]** A semiconductor device according to one embodiment of the present invention comprises a first semiconductor package, and a second semiconductor package stacked on the first semiconductor package through a

plurality of protruding electrodes having different volumes. Therefore, the thickness of the protruding electrodes between the first semiconductor package and the second semiconductor package can be adjusted, and even if there is non-uniformity in the interval between the first semiconductor package and the second semiconductor package, constrictions of the protruding electrodes can be suppressed and connection reliability between the first semiconductor package and the second semiconductor package can be enhanced.

**[0015]** Furthermore, according to one embodiment of the semiconductor device of the present invention, the volumes of the protruding electrodes are gradually changed from a central portion toward an outer peripheral portion of the semiconductor packages. Therefore, even if one or both of the first semiconductor package and the second semiconductor package warp, the first semiconductor package and the second semiconductor package can be connected while suppressing constrictions of the protruding electrodes.

**[0016]** Furthermore, according to one embodiment of the semiconductor device of the present invention, as an interval between the first semiconductor package and the second semiconductor package becomes larger, the volumes of the protruding electrodes gradually become larger. Therefore, in a region where the interval between the first semiconductor package and the second semiconductor package is large, the protruding electrodes between the first semiconductor package and the second semiconductor package can be rendered thick, and even if one or both of the first semiconductor package and the second semiconductor package warp, constrictions of the protruding electrodes between the first semiconductor

package and the second semiconductor package can be suppressed.

**[0017]** Furthermore, according to one embodiment of the semiconductor device of the present invention, the amounts of the conductive pastes of the protruding electrodes are different. Therefore, by adjusting the amounts of the conductive pastes, the thickness of the protruding electrodes between the first semiconductor package and the second semiconductor package can be adjusted, and even if there is non-uniformity in the interval between the first semiconductor package and the second semiconductor package, constrictions of the protruding electrodes can be suppressed while suppressing complication of the manufacturing process.

**[0018]** Furthermore, according to one embodiment of the semiconductor device of the present invention, the first semiconductor package comprises: a first carrier substrate; and a first semiconductor chip, flip-chip mounted on the first carrier substrate, and the second semiconductor package comprises: a second carrier substrate, mounted on the first carrier substrate through the protruding electrodes so as to be held above the first semiconductor chip; a second semiconductor chip, mounted on the second carrier substrate; and a sealing material for sealing the second semiconductor chip.

**[0019]** With this configuration, even if the first semiconductor package and the second semiconductor package are different types, the second semiconductor package can be stacked on the first semiconductor package while suppressing an increase in height, and even if there is non-uniformity in the interval between the first semiconductor package and the second semiconductor package, constrictions of the protruding electrodes can be

suppressed, so that connection reliability between the first semiconductor package and the second semiconductor package can be enhanced while saving space.

**[0020]** Furthermore, according to one embodiment of the semiconductor device of the present invention, the first semiconductor package is a ball grid array in which the first semiconductor chip is flip-chip mounted on the first carrier substrate, and the second semiconductor package is a ball grid array or a chip-size package, in which the second semiconductor chip mounted on the second carrier substrate is mold-sealed.

**[0021]** Therefore, even if generally-used packages are used, different types of packages can be stacked while suppressing constrictions of the protruding electrodes, so that connection reliability between the different types of packages can be enhanced without deteriorating production efficiency.

**[0022]** Furthermore, an electronic device according to one embodiment of the present invention comprises: a first carrier substrate, in which a plurality of first joining points are formed, the first joining points having different areas for each of the protruding electrodes; a first electronic component, flip-chip mounted on the first carrier substrate; a second carrier substrate, in which a plurality of second joining points are formed, the second joining points having different areas for each of the protruding electrodes and being arranged so as to be opposed to the first joining points; a second electronic component, mounted on the second carrier substrate; and a sealing material for sealing the second electronic component.

**[0023]** With this configuration, the second carrier substrate can be

stacked on the first carrier substrate while expansion of the protruding electrodes can be suppressed from both sides of the first carrier substrate and the second carrier substrate. Therefore, the thickness of the protruding electrodes joined between the first joining points and the second joining points can be adjusted while suppressing fluctuations of the areas of each of the joining points, and even if there is large non-uniformity in the interval between the first carrier substrate and the second carrier substrate, constrictions of the protruding electrodes can be suppressed while securing necessary areas of each of the joining points.

**[0024]** Furthermore, an electronic device according to one embodiment of the present invention comprises: a first carrier substrate; a first electronic component, flip-chip mounted on the first carrier substrate; a second carrier substrate, mounted on the first carrier substrate through a plurality of protruding electrodes having different volumes, so as to be held above the first electronic component; a second electronic component, mounted on the second carrier substrate; and a sealing material for sealing the second electronic component.

**[0025]** With this configuration, the second carrier substrate can be stacked on the first carrier substrate while expansion of the protruding electrodes can be suppressed from both sides of the first carrier substrate and the second carrier substrate. Therefore, the thickness of the protruding electrodes joined between the first joining points and the second joining points can be adjusted while suppressing fluctuations of the areas of each of the joining points, and even if there is large non-uniformity in the interval between



the first carrier substrate and the second carrier substrate, constrictions of the protruding electrodes can be suppressed while securing the areas of each of the joining points.

**[0026]** Furthermore, according to one embodiment of the semiconductor package of the present invention, areas of joining points of the protruding electrodes joined with one package are changed corresponding to warping of the other package connected to the one package. Therefore, even if the other package warps, expansion of the protruding electrodes can be suppressed on the one package side, so that thickness of the protruding electrodes joined with the one package can be adjusted on the one package side, whereby connection reliability between the packages can be enhanced.

**[0027]** Furthermore, an electronic apparatus according to one embodiment of the present invention comprises: a first semiconductor package, in which a plurality of first joining points are formed, the first joining points having different areas for each of the protruding electrodes; a second semiconductor package, in which a plurality of second joining points are formed, the second joining points having different areas for each of the protruding electrodes and being arranged so as to be opposed to the first joining points; and a motherboard, on which the first semiconductor package is mounted.

**[0028]** By changing the areas of the protruding electrodes, the thickness of the protruding electrodes joined between the first joining points and the second joining points can be adjusted, and even if there is non-uniformity in the interval between the first semiconductor package and the second semiconductor package, constrictions of the protruding electrodes can be

suppressed.

**[0029]** Furthermore, an electronic apparatus according to one embodiment of the present invention comprises: a first semiconductor package; a second semiconductor package stacked on the first semiconductor package through a plurality of protruding electrodes having different volumes; and a motherboard, on which the first semiconductor package is mounted.

**[0030]** By changing the volumes of the protruding electrodes, the thickness of the protruding electrodes between the first semiconductor package and the second semiconductor package can be adjusted, and even if there is non-uniformity in the interval between the first semiconductor package and the second semiconductor package, constrictions of the protruding electrodes can be suppressed.

**[0031]** Furthermore, a manufacturing method of a semiconductor device according to one embodiment of the present invention comprises: forming first openings having different opening areas in an insulating layer on first lands provided on a first semiconductor package; forming second openings having different opening areas in an insulating layer on second lands provided on a second semiconductor package; forming protruding electrodes on the second lands, on which the second openings are formed; and stacking the second semiconductor package on the first semiconductor package by joining the protruding electrodes formed on the second lands to the first lands.

**[0032]** With this configuration, areas of the protruding electrodes can be changed and expansion of the protruding electrodes on the lands can be controlled. Therefore, even if one or both of the first semiconductor package

and the second semiconductor package warp, the second semiconductor package can be stacked on the first semiconductor package while suppressing constrictions of the protruding electrodes.

**[0033]** Furthermore, a manufacturing method of a semiconductor device according to one embodiment of the present invention comprises: forming conductive materials having different thicknesses on a first semiconductor package by applying the conductive materials via a printing mask having a printing surface whose mask thickness varies; forming protruding electrodes on a second semiconductor package; and stacking the second semiconductor package on the first semiconductor package by joining the protruding electrodes formed on the second semiconductor package with the first semiconductor package via the conductive materials.

**[0034]** By transferring the conductive materials on the first semiconductor package with this method, the thickness of the protruding electrodes between the first semiconductor package and the second semiconductor package can be adjusted, and even if there is non-uniformity in the interval between the first semiconductor package and the second semiconductor package, constrictions of the protruding electrodes can be suppressed while suppressing complication of the manufacturing process.

**[0035]** Furthermore, a manufacturing method of a semiconductor device according to one embodiment of the present invention comprises: forming conductive materials having different thicknesses on a first semiconductor package by controlling to-be-applied amounts of the conductive materials; forming protruding electrodes on a second semiconductor package;

and stacking the second semiconductor package on the first semiconductor package by joining the protruding electrodes formed on the second semiconductor package with the first semiconductor package via the conductive materials.

**[0036]** By adjusting to-be-applied amounts of the conductive pastes (materials), the thickness of the protruding electrodes between the first semiconductor package and the second semiconductor package can be adjusted, and even if there is non-uniformity in the interval between the first semiconductor package and the second semiconductor package, constrictions of the protruding electrodes can be suppressed while suppressing complication of the manufacturing process.

**[0037]** Furthermore, a manufacturing method of an electronic device according to one embodiment of the present invention comprises: forming first openings having different opening areas in an insulating layer on first lands provided on a first carrier substrate; mounting a first electronic component on the first carrier substrate; forming second openings having different opening areas in an insulating layer on second lands provided on a second carrier substrate; mounting a second electronic component on the second carrier substrate; forming protruding electrodes on the second lands, on which the second openings are formed; and stacking the second carrier substrate on the first carrier substrate by joining the protruding electrodes formed on the second lands to the first lands.

**[0038]** With this method, the areas of the protruding electrodes can be changed, and even if one or both of the first carrier substrate and the second

carrier substrate warp, the second carrier substrate can be stacked on the first carrier substrate while suppressing constrictions of the protruding electrodes. Furthermore, a manufacturing method of an electronic device according to one embodiment of the present invention comprises: mounting a first electronic component on a first carrier substrate; forming conductive materials having different thicknesses on the first carrier substrate by applying the conductive materials via a printing mask having a printing surface whose mask thickness varies; mounting a second electronic component on a second carrier substrate; forming protruding electrodes on the second carrier substrate, on which the second electronic component is mounted; and stacking the second carrier substrate on the first carrier substrate by joining the protruding electrodes formed on the second carrier substrate with the first carrier substrate via the conductive materials.

**[0039]** By transferring the conductive materials on the first carrier substrate with this method, the thickness of the protruding electrodes between the first carrier substrate and the second carrier substrate can be adjusted, and even if there is non-uniformity in the interval between the first carrier substrate and the second carrier substrate, constrictions of the protruding electrodes can be suppressed while suppressing complication of the manufacturing process.

**[0040]** Furthermore, a manufacturing method of an electronic device according to one embodiment of the present invention comprises: mounting a first electronic component on a first carrier substrate; forming conductive materials having different thicknesses on the first carrier substrate by controlling to-be-applied amounts of the conductive materials; mounting a second

electronic component on a second carrier substrate; forming protruding electrodes on the second carrier substrate, on which the second electronic component is mounted; and stacking the second carrier substrate on the first carrier substrate by joining the protruding electrodes formed on the second carrier substrate with the first carrier substrate via the conductive materials.

**[0041]** By adjusting to-be-applied amounts of the conductive pastes (materials), the thickness of the protruding electrodes between the first carrier substrate and the second carrier substrate can be adjusted, and even if there is non-uniformity in the interval between the first carrier substrate and the second carrier substrate, constrictions of the protruding electrodes can be suppressed while suppressing complication of the manufacturing process.

#### BRIEF DESCRIPTION OF THE DRAWINGS

**[0042]** FIG. 1 shows a sectional view illustrating a constitution of a semiconductor device according to a first embodiment.

**[0043]** FIGs. 2A-C show sectional views illustrating a manufacturing method of the semiconductor device of FIG. 1.

**[0044]** FIG. 3 shows a sectional view illustrating a constitution of a semiconductor device according to a second embodiment.

**[0045]** FIGs. 4A-C show sectional views illustrating a manufacturing method of a semiconductor device according to a third embodiment.

**[0046]** FIGs. 5A-B show sectional views illustrating a manufacturing method of the semiconductor device according to a third embodiment.

**[0047]** FIGs. 6A-C show sectional views illustrating a manufacturing

method of a semiconductor device according to a fourth embodiment.

**[0048]** FIG. 7 shows a sectional view illustrating a constitution of a semiconductor device according to a fifth embodiment.

#### DETAILED DESCRIPTION

**[0049]** Hereinafter, a semiconductor device, an electronic device and a manufacturing method of the same according to embodiments of the present invention will be described referring to the drawings. FIG. 1 shows a cross-sectional view illustrating a constitution of a semiconductor device according to a first embodiment of the present invention. In the first embodiment, opening diameters of openings 13a and 13b and openings 22a and 22b for a semiconductor package PK11 and a semiconductor package PK12 respectively, with which protruding electrodes 29a and 29b are joined, are changed.

**[0050]** In FIG.1, a carrier substrate 11 is provided in the semiconductor package PK11. On a back surface of the carrier substrate 11, lands 14 for arranging protruding electrodes 19 are provided. Furthermore, on the back surface of the carrier substrate 11 provided with the lands 14, an insulating layer 12 such as a solder resist is provided, and openings 12a for exposing surfaces of the lands 14 are provided in the insulating layer 12.

**[0051]** On the other hand, on a front surface of the carrier substrate 11, lands 15a and 15b for arranging the protruding electrodes 29a and 29b, respectively, are provided, and lands 15c for arranging protruding electrodes 17 are provided. Furthermore, on the front surface of the carrier substrate 11 provided with the lands 15a through 15c, an insulating layer 13 such as a solder

resist is formed, and the openings 13a through 13c for exposing surfaces of the lands 15a through 15c are provided, respectively, in the insulating layer 13.

**[0052]** The opening diameters of the openings 13a and 13b provided corresponding to the protruding electrodes 29a and 29b, respectively, can be set, for example, so as to be gradually decreased from a central portion toward an outer peripheral portion of the carrier substrate 11. On the carrier substrate 11, a semiconductor chip 16 is flip-chip mounted, and on the semiconductor chip 16, protruding electrodes 17 for flip-chip-mounting are provided. The protruding electrodes 17 provided on the semiconductor chip 16 are ACF (Anisotropic Conductive Film) joined on the lands 15c via an anisotropic conductive film 18. On the lands 14 provided on the back surface of the carrier substrate 11, the protruding electrodes 19 for mounting the carrier substrate 11 on a motherboard are provided.

**[0053]** On the other hand, in the semiconductor package PK12, a carrier substrate 21 is provided. On a back surface of the carrier substrate 21, lands 24a and 24b for arranging the protruding electrodes 29a and 29b, respectively, are provided. Furthermore, on the back surface of the carrier substrate 21 provided with the lands 24a and 24b, an insulating layer 22 such as a solder resist is formed, and the openings 22a and 22b for exposing surfaces of the lands 24a and 24b are provided, respectively, in the insulating layer 22.

**[0054]** The opening diameters of the openings 22a and 22b provided corresponding to the protruding electrodes 29a and 29b, respectively, can be set, for example, so as to be gradually decreased from a central portion toward



an outer peripheral portion of the carrier substrate 21. On the other hand, on a front surface of the carrier substrate 11, lands 25 for wire-bonding are provided. On the front surface of the carrier substrate 21 provided with lands 25, an insulating layer 23 such as a solder resist is formed, and openings 23a for exposing surfaces of the lands 25 are provided in the insulating layer 23.

**[0055]** On the carrier substrate 21, a semiconductor chip 26a is face-up-mounted via a joining layer 27a, and the semiconductor chip 26a is wire-bonded to the lands 25 through conductive wires 28a. Furthermore, on the semiconductor chip 26a, a semiconductor chip 26b is face-up-mounted in such a manner as to avoid the conductive wires 28a, and the semiconductor chip 26b is fixed on the semiconductor chip 26a via a joining layer 27b and wire-bonded to the lands 25 through conductive wires 28b. As for the conductive wires 28a and 28b, for example, an Au wire, an Al wire or the like can be used.

**[0056]** Furthermore, on the lands 24a and 24b provided on the back surface of the carrier substrate 21, the protruding electrodes 29a and 29b for mounting the carrier substrate 21 on the carrier substrate 11 are provided, respectively, in such a manner that the carrier substrate 21 is held above the semiconductor chip 16. The protruding electrodes 29a and 29b are arranged in such a manner as to avoid a mounting region of the semiconductor chip 16, and for example, and the protruding electrodes 29a and 29b can be arranged in a peripheral portion of the back surface of the carrier substrate 21.

**[0057]** Furthermore, sealing resin 30 is provided on the whole surface of the carrier substrate 21, which is the mounting side of the semiconductor chips 26a and 26b, and the semiconductor chips 26a and 26b are sealed by the

sealing resin 30. In case that the semiconductor chips 26a and 26b are sealed by the sealing resin 30, molding using a thermosetting resin such as an epoxy resin can be employed.

**[0058]** It is assumed that a difference in coefficient of linear expansion between the carrier substrate 11 and the semiconductor chip 16 or the like causes the semiconductor package PK11 to warp downward, and a difference in coefficient of linear expansion between the carrier substrate 21 and the sealing resin 30 or the like causes the semiconductor package PK12 to warp upward. For example, in a state that the semiconductor package PK11 warps downward and the semiconductor package PK12 warps upward, by joining the protruding electrodes 29a and 29b with the lands 15a and 15b provided on the carrier substrate 11, respectively, the carrier substrate 21 can be mounted on the carrier substrate 11.

**[0059]** Both of the opening diameters of the openings 13a and 13b provided corresponding to the lower surfaces of the protruding electrodes 29a and 29b, respectively, and the openings 22a and 22b provided corresponding to the upper surfaces of the protruding electrodes 29a and 29b, respectively, are set so as to be decreased from the central portions toward the outer peripheral portions of the carrier substrates 11 and 21, respectively, and thereby, expansion of the protruding electrodes 29a and 29b can be controlled from both sides of the stacked carrier substrates 11 and 21.

**[0060]** Therefore, thickness of the protruding electrodes 29a and 29b joined between the lands 15a and 15b and the lands 24a and 24b, respectively, can be adjusted while suppressing variation amounts of areas of the protruding

electrodes 29a and 29b. Even if the warping of the carrier substrates 11 and 21 is large, constrictions of the protruding electrodes 29a and 29b can be suppressed while the areas that are required for the protruding electrodes 29a and 29b can be secured.

**[0061]** Furthermore, even in case that the carrier substrates 11 and 21 warp, by changing both of the opening diameters of the openings 13a and 13b and the openings 22a and 22b, constrictions of the protruding electrodes 29a and 29b can be suppressed without changing the volumes of the protruding electrodes 29a and 29b. Accordingly, connection reliability between the carrier substrates 11 and 21 can be enhanced while suppressing deterioration of production efficiency when the protruding electrodes 29a and 29b are formed on the carrier substrate 21.

**[0062]** For example, in case that the protruding electrodes 29a and 29b are constituted of solder balls, suppose both ball diameters thereof are set to be the same, that is, to about 0.3 mm and the warping of the carrier substrate 21 is 80  $\mu\text{m}$ . If the opening diameter of the openings 13a and 13b of the carrier substrate 11 are rendered constant at about 0.3 mm and the opening diameter of the openings 24b in the central portion of the carrier substrate 21 are set to about 0.28 mm, a mounting height at the central portion of the carrier substrate 21 is 0.205 mm. In this case, the opening diameter of the openings 24a at an end portion of the carrier substrate 21 needs to be set to about 0.05 mm in order that a mounting height at the end portion of the carrier substrate 21 is 0.285 mm. Therefore, the opening diameter of the openings 24a becomes extremely small and the area of the protruding electrodes 29a and lands 24a

becomes too small, thereby leading to a deficiency of the joining strength of the protruding electrodes 29a and the lands 24a.

**[0063]** On the other hand, if the opening diameter of the openings 13a at an end portion of the carrier substrate 11 is set to about 0.28 mm so as to be smaller while maintaining the opening diameter of the openings 13b at a central portion of the carrier substrate 11 at about 0.3 mm, the opening diameter of the openings 24a at the end portion of the carrier substrate 21 may be set to about 0.25 mm in order that the mounting height at the end portion of the carrier substrate 21 is 0.285 mm. Therefore, the opening diameter of the openings 24a is prevented from being too small while a necessary mounting height can be secured.

**[0064]** In addition, as for the carrier substrates 11 and 21, for example, a double-sided substrate, a multilayer-interconnection substrate, a build-up substrate, a tape substrate, or a film substrate or the like can be used. As for the material of the carrier substrates 11 and 21, for example, a polyimide resin, a glass epoxy resin, BT resin, a composite of aramid and epoxy, or a ceramic or the like can be used. Moreover, as for the protruding electrodes 16, 19, 29a, and 29b, for example, Au bump, Cu bump and Ni bump covered with a solder material or the like, or a solder ball can be used. In particular, for the protruding electrodes 29a and 29b, a solder ball, conductive paste or the like is preferably used. Furthermore, although the method of providing the protruding electrodes 29a and 29b on the side of the carrier substrate 21 in order to mount the carrier substrate 21 on the carrier substrate 11 is described, the protruding electrodes 29a and 29b may be provided on the side of the carrier substrate 11.

**[0065]** Furthermore, although in the above-described embodiment, the method of mounting the semiconductor chip 16 on the carrier substrate 11 by ACF joining is described, for example, other pressure-welding joining such as ACF joining, NCF (Nonconductive Film) joining, ACP (Anisotropic Conductive Paste) joining, and NCP (Nonconductive Paste) joining may be used, and metal joining such as solder joining and alloy joining may also be used. In case that the semiconductor chips 26a and 26b are mounted on the carrier substrate 21, although the method of using wire-bonding is described, the semiconductor chips 26a and 26b may be flip-chip mounted on the carrier substrate 21. Furthermore, although in the above-described embodiment, the method of mounting one semiconductor chip 16 on the carrier substrate 11 is described as an example, a plurality of semiconductor chips may be mounted on the carrier substrate 11. Still further, a resin may be injected into a gap between the carrier substrates 11 and 21 as required. In addition, although in the above-described embodiment, an example of face-down-mounting of the semiconductor chip 16 on the carrier substrate 11 is described, it may be face-up-mounted (not shown). In this case, the semiconductor chip 16 may be sealed. Furthermore, in this case, the shape of a portion of the carrier substrate 11 where the semiconductor chip 16 is sealed is modified into a downward convex shape and the shape of a portion where the semiconductor chip is not sealed is modified into an upward convex shape.

**[0066]** Furthermore, although in the above-described embodiment, a case that the lower carrier substrate 11 warps downward and the upper carrier substrate 21 warps upward is described as an example, the embodiment can be

similarly applied to a case that the lower carrier substrate 11 does not warp and the upper carrier substrate 21 warps upward, a case that the upper carrier substrate 21 does not warp and the lower carrier substrate 11 warps downward, a case that both of the carrier substrates 11 and 21 warp downward and the lower carrier substrate 11 warps more largely, and a case that both of the carrier substrate 11 and 21 warp upward and the upper carrier substrate 21 warps more largely.

**[0067]** Furthermore, the embodiment may be applied to a case that the lower carrier substrate 11 warps upward and the upper carrier substrate 21 warps downward, a case that the lower carrier substrate 11 does not warp and the upper carrier substrate 21 warps downward, a case that the upper carrier substrate 21 does not warp and the lower carrier substrate 11 warps upward, a case that both of the carrier substrates 11 and 21 warp downward and the upper carrier substrate 11 warps more largely, and a case that both of the carrier substrates 11 and 21 warp upward and the lower carrier substrate 21 warps more largely. In these cases, both of the opening diameters of the openings 13a and 13b provided corresponding to the lower surfaces of the protruding electrodes 29a and 29b, respectively, and the openings 22a and 22b provided corresponding to the upper surfaces of the protruding electrodes 29a and 29b, respectively are preferably set so as to be increased from the central portions to the peripheral portions of the carrier substrates 11 and 21, respectively.

**[0068]** FIGs. 2A-C show cross-sectional views illustrating a manufacturing method of the semiconductor of FIG. 1. In FIG. 2 (a), the semiconductor package PK11 warps downward and the semiconductor package

PK12 warps upward. In case that the semiconductor package PK12 is stacked on the semiconductor package PK11, the protruding electrodes 29a and 29b are formed on the lands 24a and 24b of the carrier substrate 22, respectively. In case that solder balls are used for the protruding electrodes 29a and 29b, for example, diameters of the balls can be set to substantially the same (that is, within a range of a manufacturing variance).

**[0069]** Next, as shown in FIG. 2 (b), the semiconductor package PK12 with the protruding electrodes 29a and 29b formed is mounted on the semiconductor package PK11 and subjected to reflow process to join the electrodes 29a and 29b with the lands 15a and 15b, and the lands 24a and 24b, respectively. By setting both of the opening diameters of the openings 13a and 13b provided corresponding to the lower surfaces of the protruding electrodes 29a and 29b, and the openings 22a and 22b provided corresponding to the upper surfaces of the protruding electrodes 29a and 29b so as to be decreased from the central portions to the peripheral portions of the carrier substrates 11 and 21, even if the solder ball having the same diameters are used as the protruding electrodes 29a and 29b, the mounting height of the carrier substrate 21 can be matched with the warping of the carrier substrates 11 and 21 while suppressing constrictions of the protruding electrodes 29a and 29b.

**[0070]** Next, as shown in FIG. 2 (c), the protruding electrodes 19 for mounting the carrier substrate 11 on the motherboard are formed on the lands 14 provided on the back surface of the carrier substrate 11.

**[0071]** FIG. 3 shows a cross-sectional view illustrating a constitution of a semiconductor device according to a second embodiment of the present

invention. In the second embodiment, opening diameters of openings 43a and 43b and openings 52a and 52b of semiconductor packages PK21 and PK22, with which protruding electrodes 59a and 59b are joined, are changed, respectively, and opening diameters of openings 42a through 42c of the semiconductor package PK21, with which protruding electrodes 49a to 49c are joined, are changed.

**[0072]** In FIG. 3, a carrier substrate 41 is provided in the semiconductor package PK21. On a back surface of the carrier substrate 41, lands 44a through 44c for arranging the protruding electrodes 49a through 49c are provided. Furthermore, on the back surface of the carrier substrate 41 provided with the lands 44a through 44c, an insulating layer 42 such as a solder resist is provided, and the openings 42a through 42c for exposing surfaces of the lands 44a through 44c are provided in the insulating layer 42.

**[0073]** The opening diameters of the openings 42a through 44c provided corresponding to the protruding electrodes 49a through 49c, respectively, can be set, for example, so as to be gradually increased from a central portion toward an outer peripheral portion of the carrier substrate 41. On the other hand, on a front surface of the carrier substrate 41, lands 45a and 45b for arranging the protruding electrodes 59a and 59b are provided, respectively, and lands 45c for arranging protruding electrodes 47 are provided. Furthermore, on the front surface of the carrier substrate 41 provided with the lands 45a, 45b and 45c, an insulating layer 43 such as a solder resist is formed, and the openings 43a through 43c for exposing surfaces of the lands 45a through 45c are provided, respectively, in the insulating layer 43.



**[0074]** The opening diameters of the openings 43a through 43b provided corresponding to the protruding electrodes 59a through 59b, respectively, can be set, for example, so as to be gradually decreased from the central portion toward the outer peripheral portion of the carrier substrate 41. On the carrier substrate 41, a semiconductor chip 46 is flip-chip mounted, and on the semiconductor chip 46, protruding electrodes 47 for the flip-chip-mounting are provided. The protruding electrodes 47 provided on the semiconductor chip 43 are ACF joined on the lands 45c via an anisotropic conductive film 48. On the lands 44a through 44c provided on the back surface of the carrier substrate 41, the protruding electrodes 49a through 49c for mounting the carrier substrate 41 on a motherboard 71 are provided.

**[0075]** On the other hand, in the semiconductor package PK22, a carrier substrate 51 is provided. On a back surface of the carrier substrate 51, lands 54a and 54b for arranging the protruding electrodes 59a and 59b are provided, respectively. Furthermore, on the back surface of the carrier substrate 51 provided with the lands 54a and 54b, an insulating layer 52 such as a solder resist is formed, and the openings 52a and 52b for exposing surfaces of the lands 54a and 54b are provided, respectively, in the insulating layer 52.

**[0076]** The opening diameters of the openings 52a and 52b provided corresponding to the protruding electrodes 59a and 59b, respectively, can be set, for example, so as to be gradually decreased from a central portion toward an outer peripheral portion of the carrier substrate 51. On the other hand, on a front surface of the carrier substrate 51, lands 55 for wire-bonding are provided.

On the front surface of the carrier substrate 51 provided with lands 55, an insulating layer 53 such as a solder resist is formed, and openings 53a for exposing surfaces of the lands 55 are provided in the insulating layer 53.

**[0077]** On the carrier substrate 51, a semiconductor chip 56a is face-up-mounted via a joining layer 57a, and the semiconductor chip 56a is wire-bonded to the lands 55 via conductive wires 58a. Furthermore, on the semiconductor chip 56a, a semiconductor chip 56b is face-up-mounted in such a manner as to avoid the conductive wires 58a, and the semiconductor chip 56b is fixed on the semiconductor chip 56a via a joining layer 57b and wire-bonded to the lands 55 through conductive wires 58b.

**[0078]** Furthermore, on the lands 54a and 54b provided on the back surface of the carrier substrate 51, the protruding electrodes 59a and 59b are provided for mounting the carrier substrate 51 on the carrier substrate 41 in such a manner that the carrier substrate 51 is held above the semiconductor chip 46. The protruding electrodes 59a and 59b are arranged in such a manner as to avoid a mounting region of the semiconductor 46, and for example, the protruding electrodes 59a and 59b can be arranged in a peripheral portion of the back surface of the carrier substrate 51.

**[0079]** Furthermore, sealing resin 60 is provided on the whole surface of the carrier substrate 51, which is the mounting side of the semiconductor chips 56a and 56b, and the semiconductor chips 56a and 56b are sealed by the sealing resin 60. It is assumed that a difference in coefficient of linear expansion between the carrier substrate 41 and the semiconductor chip 46 or the like causes, for example, the semiconductor package PK21 to warp

downward, and a difference in coefficient of linear expansion between the carrier substrate 51 and the sealing resin 60 or the like causes the semiconductor package PK22 to warp upward.

**[0080]** For example, in the state that the semiconductor package PK21 warps downward and the semiconductor package PK22 warps upward, by joining the protruding electrodes 59a and 59b with the lands 45a and 45b provided on the carrier substrate 41, respectively, the carrier substrate 51 can be mounted on the carrier substrate 41. Furthermore, by joining the protruding electrodes 49a through 49c with lands 72 provided on the motherboard 71, the carrier substrate 11 with the carrier substrate 21 stacked can be mounted on the motherboard 71.

**[0081]** Both of the opening diameters of the openings 43a and 43b provided corresponding to the lower surfaces of the protruding electrodes 59a and 59b, respectively, and the openings 52a and 52b provided corresponding to the upper surfaces of the protruding electrodes 59a and 59b, respectively, are set so as to be decreased from the central portions toward the outer peripheral portions of the carrier substrates 41 and 51, respectively, and thereby, expansion of the protruding electrodes 59a and 59b can be controlled from both sides of the stacked carrier substrates 41 and 51.

**[0082]** Therefore, thickness of the protruding electrodes 59a and 59b joined between the lands 45a and 45b and the lands 54a and 54b, respectively, can be adjusted while suppressing variation amount of areas of the protruding electrodes 59a and 59b. Even in case that the warping of the carrier substrates 41 and 51 is large, constrictions of the protruding electrodes 59a and 59b can

be suppressed while the areas that are required for the protruding electrodes 59a and 59b can be secured.

**[0083]** Furthermore, in the carrier substrate 41 interposed between the carrier substrate 51 and the motherboard 71, even in case that the carrier substrate 41 warps, by changing not only the opening diameters of the openings 43a and 43b provided in the one surface but also the diameters of the openings 42a and 42b provided in the other surface, not only constrictions of the protruding electrodes 59a and 59b joined with the carrier substrate 51 but also constrictions of the protruding electrodes 49a through 49c joined with the motherboard 71 can be suppressed. Accordingly, not only connection reliability between the carrier substrate 41 and the carrier substrate 51 can be enhanced but also connection reliability between the carrier substrate 41 and the motherboard 71 can be enhanced.

**[0084]** In addition, as for the carrier substrates 41 and 51 and the motherboard 71, for example, a double-sided substrate, a multilayer-interconnection substrate, a build-up substrate, a tape substrate, or a film substrate or the like can be used. As for the material of the carrier substrates 41 and 51 and the motherboard 71, for example, a polyimide resin, a glass epoxy resin, BT resin, a composite of aramid and epoxy, or a ceramic or the like can be used. Moreover, as for the protruding electrodes 46, 49a through 49c, 59a and 59b, for example, Au bump, Cu bump and Ni bump covered with a solder material or the like, or a solder ball can be used. In particular, for the protruding electrodes 49a through 49c, 59a and 59b, a solder ball, conductive paste or the like is preferably used. Furthermore, although in the above-

described embodiment, a case that the lower carrier substrate 41 warps downward and the upper carrier substrate 51 warps upward is described as an example, the embodiment can be similarly applied to a case that the upper carrier substrate 51 does not warp and the lower carrier substrate 41 warps downward, and a case that both of the carrier substrates 41 and 51 warp downward and the lower carrier substrate 41 warps more largely.

**[0085]** Furthermore, in case that the lower carrier substrate 41 warps upward, with or without warping of the upper carrier substrate 51, the opening diameters of the openings 42a through 44c provided corresponding to the protruding electrodes 49a through 49c, respectively, can be set so as to be gradually decreased from the central portion toward the outer peripheral portion of the carrier substrate 41.

**[0086]** FIGs. 4A-C and FIGs. 5A-B show cross-sectional views illustrating a manufacturing method of a semiconductor device according to a third embodiment of the present invention. In the third embodiment, by changing a mask thickness of a printing mask 111, thickness of conductive pastes 89a and 89b printed on a carrier substrate 81 are adjusted.

**[0087]** In FIG. 4, a carrier substrate 81 is provided in a semiconductor package PK31. On a back surface of the carrier substrate 81, lands 84 for arranging protruding electrodes 102 of FIG. 5 (b) are provided. Furthermore, on the back surface of the carrier substrate 11 provided with the lands 84, an insulating layer 82 is provided, and openings 82a for exposing surfaces of the lands 84 are provided the insulating layer 82.

**[0088]** On the other hand, on a front surface of the carrier substrate

81, lands 85a and 85b for joining protruding electrodes 101a and 101b of FIG. 5 (a) are provided, respectively, and lands 85c for arranging protruding electrodes 87 are provided. Furthermore, on the front surface of the carrier substrate 81 provided with the lands 85a through 85c, an insulating layer 83 is formed, and openings 83a through 83c for exposing surfaces of the lands 85a through 85c are provided, respectively, in the insulating layer 83. Opening diameters of the openings 83a through 83c can be set so as to be substantially the same.

**[0089]** On the carrier substrate 81, a semiconductor chip 86 is flip-chip mounted, and on the semiconductor chip 86, protruding electrodes 87 for flip-chip-mounting are provided. The protruding electrodes 87 provided on the semiconductor chip 86 are ACF joined on the lands 85c via an anisotropic conductive film 88. On the other hand, in a semiconductor package PK32, a carrier substrate 91 is provided. On a back surface of the carrier substrate 91, lands 94a and 94b for arranging protruding electrodes 99a and 99b are provided, respectively. Furthermore, on the back surface of the carrier substrate 91 provided with the lands 94a and 94b, an insulating layer 92 is provided, and openings 92a and 92b for exposing surfaces of the lands 94a and 94b are provided, respectively, in the insulating layer 92. Opening diameters of the openings 92a and 92b can be set so as to be substantially the same.

**[0090]** On the other hand, on a front surface of the carrier substrate 91, lands 95 for wire-bonding are provided. On the front surface of the carrier substrate 91 provided with the lands 95, an insulating layer 93 is formed, and openings 93a for exposing surfaces of the lands 95 are provided in the insulating layer 93. On the carrier substrate 91, a semiconductor chip 96a is

face-up-mounted via a joining layer 97a, and the semiconductor chip 96a is wire-bonded to the lands 95 through conductive wires 98a. Furthermore, on the semiconductor chip 96a, a semiconductor chip 96b is face-up-mounted in such a manner as to avoid the conductive wires 98a, and the semiconductor chip 96b is fixed on the semiconductor chip 96a via a joining layer 97b and wire-bonded to the lands 95 through conductive wires 98b.

**[0091]** Furthermore, on the lands 94a and 94b provided on the back surface of the carrier substrate 91, the protruding electrodes 99a and 99b are provided for mounting the carrier substrate 91 on the carrier substrate 81 in such a manner that the carrier substrate 91 is held above the semiconductor chip 86. Furthermore, sealing resin 100 is provided on the whole surface of the carrier substrate 91, which is the mounting side of the semiconductor chips 96a and 96b, and the semiconductor chips 96a and 96b are sealed by the sealing resin 100.

**[0092]** On the other hand, openings 113a and 113b for charging conductive pastes 89 are provided in the printing mask 111, and an opening 112, in which the semiconductor chip 86 can be inserted, is provided on the side of a transfer surface of the printing mask 111. The mask thickness of the printing mask 111 can be set so as to be changed according to positions of the openings 113a and 113b, for example, so as to be gradually increased from a central portion toward an outer peripheral portion of the printing mask 111.

**[0093]** For example, in case that the mask thickness of the printing mask 111 is changed, a cross-sectional shape of the printing mask 111 on the transfer surface side can be an arch while keeping a cross-sectional shape of

an upper surface of the printing mask 111 flat. It is assumed that the semiconductor package PK31 warps downward and the semiconductor package PK32 warps upward. In case that the semiconductor package PK32 is stacked on the semiconductor package PK31, the conductive pastes 89 are supplied on the upper surface of the printing mask 111. After charging the conductive pastes 89 to the openings 113a and 113b of the printing mask 111, respectively, the carrier substrate 81 is pressed to the printing mask 111. Furthermore, by moving a squeegee 114 on the printing mask 111 to which the conductive pastes 89 are supplied, the conductive pastes 89 are charged to the openings 113a and 113b. By gradually increasing the mask thickness from the central portion toward the outer peripheral portion of the printing mask 111, a charging amount of the openings 113a arranged in the end portion can be larger than that of the openings 113b arranged in the central portion.

**[0094]** As shown in FIG. 4 (b), the conductive pastes 89 charged to the openings 113a and 113b of the printing mask 111 are transferred on the lands 85a and 85b of the carrier substrate 81 to print the conductive pastes 89a and 89b on the lands 85a and 85b of the carrier substrate 81, respectively. The charging amount of the conductive pastes 89 charged in the openings 113a is larger than that of the conductive pastes 89 charged in the openings 113b. Therefore, a thickness of the conductive pastes 89a of the lands 85a of the carrier substrate 81 can be larger than that of the conductive pastes 89b on the lands 85b.

**[0095]** Next, as shown in FIG. 4 (c), the semiconductor package PK32, in which the protruding electrodes 99a and 99b are formed, is mounted



on the semiconductor package PK31, on which the conductive pastes 89a and 89b are printed. Next, as shown in FIG. 5 (a), the conductive pastes 89a and 89b and the protruding electrodes 99a and 99b are melted by reflow process. In this manner, the protruding electrodes 101a and 101b made of the conductive pastes 89a and 89b and the protruding electrodes 99a and 99b are joined onto the lands 85a and 85b and the lands 94a and 94b, respectively.

**[0096]** This enables the conductive pastes 89a and 89b to be integrally formed on the lands 85a and 85b of the carrier substrate 81 while volumes of the protruding electrodes 101a and 101b can be changed corresponding to an interval between the carrier substrate 81 and the carrier substrate 91. Accordingly, even if the carrier substrates 81 and 91 warp, constrictions of the protruding electrodes 101a and 101b can be suppressed, and connection reliability between the carrier substrates 81 and 91 can be enhanced while suppressing deterioration in production efficiency.

**[0097]** Next, as shown in FIG. 5 (b), the protruding electrodes 89 for mounting the carrier substrate 81 on a motherboard are formed on the lands 84 provided on the back surface of the carrier substrate 81.

**[0098]** FIGs. 6A-C show cross-sectional views illustrating a manufacturing method of a semiconductor device according to a fourth embodiment of the present invention. In the fourth embodiment, by adjusting to-be-applied amount of the conductive pastes 89, the thickness of the conductive pastes 89a and 89b applied to the carrier substrate 81 are adjusted.

**[0099]** In FIG. 6, in case that the conductive pastes 89a and 89b are formed on the lands 85a and 85b of the carrier substrate 81, a dispenser 121 is

used. The conductive pastes 89a and 89b are formed on the lands 85a and 85b of the carrier substrate 81 while adjusting the supplying amount of the conductive pastes 89 for the each of the lands 85a and 85b. This enables volumes of the protruding electrodes 101a and 101b to be changed corresponding to an interval between the carrier substrate 81 and the carrier substrate 91. Accordingly, even if the carrier substrates 81 and 91 warp, constrictions of the protruding electrodes 101a and 101b can be suppressed.

**[0100]** FIG. 7 shows a cross-sectional view illustrating a constitution of a semiconductor device according to a fifth embodiment of the present invention. In the fifth embodiment, opening diameters of openings 226a and 226b provided corresponding to protruding electrodes 227a and 227b of a W-CSP (Wafer-level Chip-Size Package) are changed. In FIG. 7, a carrier substrate 211 is provided in a semiconductor package PK41. On a back surface of the carrier substrate 211, lands 214 for arranging protruding electrodes 219 are provided. Furthermore, on the back surface of the carrier substrate 211 provided with the lands 214, an insulating layer 212 such as a solder resist is provided, and openings 212a for exposing surfaces of the lands 214 are provided in the insulating layer 212.

**[0101]** On the other hand, on a front surface of the carrier substrate 211, lands 215a and 215b for arranging protruding electrodes 229a and 229b are provided, respectively, and lands 215c for arranging protruding electrodes 217 are provided. Furthermore, on the front surface of the carrier substrate 211 provided with the lands 215a through 215c, an insulating layer 213 such as a solder resist is formed, and the openings 213a through 213c for exposing

surfaces of the lands 215a through 215c are provided, respectively, in the insulating layer 213.

**[0102]** Opening diameters of the openings 213a and 213b provided corresponding to the protruding electrodes 229a and 229b, respectively, can be set, for example, so as to be gradually decreased from a central portion toward an outer peripheral portion of the carrier substrate 211. On the carrier substrate 211, a semiconductor chip 216 is flip-chip mounted, and on the semiconductor chip 216, the protruding electrodes 217 for flip-chip-mounting are provided. The protruding electrodes 217 provided on the semiconductor chip 216 are ACF joined on the lands 215c via an anisotropic conductive film 218. On the lands 214 provided on the back surface of the carrier substrate 211, the protruding electrodes 219 for mounting the carrier substrate 211 on a motherboard are provided.

**[0103]** On the other hand, in a semiconductor package PK42, a semiconductor chip 221 is provided. On the semiconductor chip 221, electrode pads 222 are provided, and an insulating layer 223 are provided in such a manner so as to expose the electrode pads 222. On the semiconductor chip 221, a stress-relieving layer 224 is provided in such a manner so as to expose the electrode pads 222. On the electrode pads 222, re-routing wirings 225 is formed while extending on the stress-relieving layer 224, and on the stress-relieving layer 224, lands 225a and 225b for arranging the protruding electrodes 227a and 227b, respectively, are formed. Furthermore, on the re-routing wirings 225 and the lands 225a and 225b, a solder resist film 226 is formed, and openings 226a and 226b for exposing the lands 225a and 225b on the stress-

relieving layer 224, respectively, are formed in the solder resist film 226.

**[0104]** Opening diameters of the openings 226a and 226b provided corresponding to the protruding electrodes 227a and 227b, respectively, can be set, for example, so as to be gradually decreased from a central portion toward an outer peripheral portion of the semiconductor chip 221. On the lands 225a and 225b exposed through the openings 226a and 226b, the protruding electrodes 227a and 227b are provided, respectively, for face-down-mounting the semiconductor chip 221 in such a manner that the semiconductor chip 221 is held above the semiconductor chip 216. The protruding electrodes 227a and 227b can be arranged in such a manner so as to avoid a mounting region of the semiconductor chip 216. For example, the protruding electrodes 227a and 227b can be arranged in a peripheral portion of the semiconductor chip 221.

**[0105]** It is assumed that a difference in coefficient of linear expansion between the carrier substrate 211 and the semiconductor chip 216 or the like causes, for example, the semiconductor package PK41 to warp downward, and a difference in coefficient of linear expansion between the semiconductor chip 221 and the stress-relieving layer 224 or the like also causes the semiconductor package PK 42 to warp downward and the semiconductor package PK41 to warp more largely than the semiconductor package PK42.

**[0106]** For example, in a state that the semiconductor package PK41 warps downward, the semiconductor package PK42 also warps downward, and the semiconductor package PK41 warps more largely than the semiconductor package PK42, by joining the protruding electrodes 227a and 227b with the lands 215a and 215b provided on the carrier substrate 211, respectively, the

semiconductor chip 221 can be mounted on the carrier substrate 211. Although in the above-described example, the semiconductor package PK41 warps more largely than the semiconductor package PK42, the semiconductor package 42 may warp more largely than the semiconductor package 41.

**[0107]** Thereby, the W-CSP can be stacked on the carrier substrate 211, on which the semiconductor chip 216 is flip-chip mounted, and the semiconductor chip 221 is three-dimensionally mounted above the semiconductor chip 216 without interposing any carrier substrate between the semiconductor chips 216 and 221 even in case that the semiconductor chips 216 and 221 are different in type or size. Furthermore, expansion of the protruding electrodes 227a and 227b can be suppressed from both sides of the carrier substrate 211 and the semiconductor chip 221.

**[0108]** Therefore, even in case that the semiconductor package PK41 and PK42 warp, constrictions of the protruding electrodes 227a and 227b can be suppressed while suppressing an increase in height when stacking the semiconductor chips 216 and 221, so that space can be saved when mounting the semiconductor chips 216 and 221 while suppressing deterioration of connection reliability in the three-dimensional mounting.

**[0109]** Although in the above-described embodiment, a case that the opening diameters of the openings 226a and 226b are gradually decreased from the central portion toward the outer peripheral portion of the semiconductor chip 221 is described, in case that the semiconductor package PK42 warps downward, the opening diameters of the openings 226a and 226b may be set so as to be gradually increased from the central portion toward the outer

peripheral portion of the semiconductor chip 221.

**[0110]** Furthermore, the above-described semiconductor devices and electronic devices can be applied to electronic apparatuses such as, for example, liquid crystal display device, cellular phone, personal digital assistant, video camera, digital camera, MD (Mini Disc) player or the like. And reliability of these electronic apparatuses can be enhanced while realizing downsizing and weight savings in the electronic apparatuses. Furthermore, although in the above-described embodiments, the methods of mounting the semiconductor chips or the semiconductor packages are described as examples, the present invention is not limited to the methods of mounting the semiconductor chips or the semiconductor packages. For example, ceramic elements such as a surface acoustic wave (SAW) element, optical elements such as an optical modular and optical switch, various sensors such as a magnetic sensor and bio-sensor or the like may be mounted.